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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,299	08/27/2001	Kent Wendorf	81862.P238	5134

7590 12/12/2003

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 12/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,299	WENDORF ET AL.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-57 have been examined.

Drawings

2. Figure 3 is objected to as failing to comply with 37 CFR 1.84(p)(5) because it does not include the following reference sign(s) mentioned in the description: Page 10, line 7 identifies "a compare equal 350". This reference sign is missing from Figure 3.

3. Figure 4 is objected to because of incorrect labeling of the PCI Communications Link Master (PCLM) 400 as disclosed in the specification. Figure 7 has the label PECLM 400 and the specification identifies as PCLM 400. Correct drawing for consistent labeling with the specification.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

5. Reference to the "bus slave controller" is inconsistent throughout the specification. On page 3, paragraph 3, lines 3, 4, a bus slave controller" is disclosed. On pages 5, a "slave bus controller" is discussed and on page 6 a "slave bus controller 250" is disclosed in reference to Figure 2 which shows a UBS 250. Page 7, paragraph 13, line 7 refers to a "Utility Bus Slave 250" and is referred to as the Utility Bus Slave for the

balance of the specification (Page 7, Paragraph 14, line 5; Page 9, paragraph 18, lines 2, 3). Correction for consistency is required. It is the examiners suggestion that all occurrences should be changed to "Utility Bus Slave 250" so Figure 2 does not have to be modified.

6. The labeling of the memory controller(s) is inconsistent and confusing. On page 9 it is label as "memory controller 270", "memory controllers 270", "memory controllers 430", and "memory controller 270/430". Correction for consistency or clarification is required. In addition, the labeling of the "memory controller 255" on page 10, line 3, is in error. Appropriate corrections are required.

7. The naming of block 328 in Figure 3 is inconsistent in the specification. It is named as follows:

- Memory done signal 328 (page 8, Para. 15, line 7)
- Done 328 (page 9, Para. 18, line 17)
- The done signal 328 (page 10, Para. 19, line 13)
- The data transfer is complete 328 (page 10, Para. 19, line 15)

Appropriate naming corrections for consistency and clarity are required.

8. The phrase "address in incremented" should be changed to "address is incremented" on page 10, Para. 20, line 5.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 10, 11, 24, 25, 38, 39 52, 53 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The single address mode (claims 10, 24, 38, 52) is not described in the specification.

The burst/block mode (Claims 11, 25, 39, 53) is not described in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 2, 4, 11, 17, 25, 31, 39, and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2:

Claim 2 discloses in line 6, "the second memory testing engine controlled by the processor via the bus;". Because claim 2 is dependent on claim 1, the examiner assumes this bus is the one disclosed in claim1. The disclosure in claim 2 describes direct connectivity between the processor and the second memory testing engine, however, the bus in line 10 of claim 1 connects the processor to the bus slave controller not the memory testing engine. It is requested that the applicant address these issues and make appropriate corrections concerning the connection between the processor and memory test engine or supply further disclosure of the nature of this claim.

Claims 4:

The term "slave bus controller" should be replaced with "bus slave controller".

Claims 11, 25, 39, 53:

The term "burst/block mode" is indefinite. In addition, claim should be written to reflect burst or block mode since these are two different operations. It doesn't describe how the test engine tests the memory in either the burst mode or block mode.

Claims 17:

At line 5, it is not clear whether a single RAM or plurality of RAMS are being tested due to the phrase "testing a random access memories" (plural).

Claims 17, 31:

The above claims discloses "a plurality of memory testing engines, each coupled to an application specific integrated circuit via a bus slave controller; and testing a random access memories associated with the integrated circuit using the memory testing engine." These claims are indefinite because they do not disclose which memory

test engine of the plurality to test which integrated circuit. Clarification and correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claim 1, 4, 5-8, 10, 12, 13, 16, 19-22, 24, 26, 27, 30, 33-36, 38, 40, 41, 44, 47-50, 52, 54, 55 rejected under 35 U.S.C. 102(b) as being anticipated by Miner (US-6370661 B1).

Claim 1:

Miner teaches of testing memory circuits 510 in a microprocessor, which includes a bus unit 530 that controls a normal bus 554, test management logic 570 interfaces to test execution logic 560. The test execution logic is coupled to the test management logic and executes the specific test program. The test execution logic 560 directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed. The test management logic 570 accepts test parameters in a configuration register 572 that are transferred from the test controller 580 over the test control bus 575. (See col. 6, lines, 63-67; col. 7, lines 1-4, col. 2, lines 42, 43, col. 10, lines, 12-15, 61-63).

Claims 16, 44:

The test management logic 570 communicates with a test controller 580 over the test control bus 575. The test execution logic 560 directly interfaces to the bus controller 530, the test management logic 570 and the memories 510, thereby allowing the memories 510 to be tested. (See col. 10, lines 8-15).

Claim 30:

Miner teaches the use of a ROM to store test sequences and pass them from the test controller 580 to the test execution logic 560 via bus 574 for perform memory testing. (See Col. 11, lines 5-20)

Claim 4:

Miner teaches the test execution logic 560 directly interfaces to the memories 510 and to the bus controller 530.

Claim 5, 19, 33, 47:

Miner teaches the test execution logic 560 executes test sequences of data patterns to write and expected data patterns to read. (See col. 10, lines 49-54, col. 11, lines 12-18).

Claims 6, 20, 34, 48:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 27-29).

Claims 10, 24, 38, 52:

Miner teaches that the test execution logic 560 to directly drives address, data, and control signals on the local bus 532 to directly access each of the memories 510. More specifically, address logic 561 in the test execution logic 560 generates addresses for specified locations in a memory 510 and provides these addresses directly to the

local bus 532. (See col. 10, lines 26-33). Miner further discloses that the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54).

Claims 21, 35, 49:

Miner teaches the test sequences that are designed into the test management logic 570 can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. In addition, a test sequence can be configured to repeat a specified number of times before it completes. (See col. 10, lines 49-56). Miner also teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 26-28).

Claims 7, 8, 22, 36, 50:

Miner teaches the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing,

start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18).

Claims 12,13, 26, 27,40, 41, 54, 55:

Miner teaches that the result of each read, containing a bit-by-bit result, is provided to the test management logic 570 via bus 574. The result is placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 28-31 and col. 10, lines 56-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 9, 11, 15, 17, 23, 25, 29, 31, 37, 39, 43, 45, 51, 53 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1).

Claims 2, 45:

Miner does not explicitly teach of a second memory test engine to test a second random access memory. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the teaching of Miner can be duplicated

to include a second test execution logic and test management logic entities to perform a similar function.

Claims 17, 31:

Miner does not explicitly teach of a plurality of memory test engines to test a random access memory. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the teaching of Miner can be duplicated to include a plurality of test execution logic and test management logic entities to perform a similar function. The artisan would have been motivated to do so because duplicate parts for multiple effects depend on the necessity of time saving for testing the memories.

Claims 15, 29, 43, 57:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern. Any detected defects are represented by a mask bit (logical "1") and placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 24-31, 44, 45). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the mask bit set in the result register alerts the test controller of the mismatch and alters operation.

Claims 9, 23, 37, 51:

Miner teaches the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory

510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18). Miner does not explicitly disclose that the address is decremented, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the configurable test sequences within the test management logic 570 that can access to any memory 510, within any address range, in an incrementing order can also decrement the address in testing the memory. The artisan would be motivated to do so since it is common practice in testing memories to decrement as well as increment the address locations.

Claims 11, 25, 39, 53:

Miner does not explicitly teach the block mode. Miner, however, teaches that data can be read or written within any address range (col. 10, lines 49-54). It would have been obvious to one skilled in the art at the time the invention was made to realize that Miner's "any address range" would have been a block of memory. The artisan would have been motivated to do so because Miner's address range (col. 10, line 54) does not exclude to the inclusion of reading a whole block of memory.

13. Claims 3, 18, 32, 46 rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Satoh (US-6501690 B2).

Claims 3, 18, 32, 46:

Miner does not explicitly teach that the test execution logic performs testing concurrently. However, Miner does teach the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18). Satoh teaches of a method for diagnosing a memory array including a plurality of memory banks, which can independently read/write data by writing identical data in parallel. This method also reads out storage data and compares the data read out to the data that was written. According to the above method, the memory including the plurality of banks can be diagnosed at one time or concurrently. (See col. 1, 43-48, 54, 55). Satoh also teaches the memory diagnostic circuit controls the memory banks to collectively write data at one time, and the comparison circuit compares the written data and the data from the memory banks. In this structure, the plurality of memory banks can be diagnosed at one time. (See col. 2, lines 6-12). Also, in the memory diagnostic circuit 11 of this embodiment, the plurality of memories 14a to 14d, which are divided into four memory banks, can collectively be diagnosed at one time. (See col. 5, lines 65-67, col. 6, line 1). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to "reconfigure" the test sequences within the test management logic of Miner to test the memories concurrently in view of the teachings of Satoh. Specifically, the control logic within the test execution logic directly generates control signals over a memory control bus to select and control a specified memory. The artisan would have a motivation to do so because Miner suggests that the test controller can access many memories (see col. 10, lines 49-54) which would be more than one memory.

14. Claims 14, 28, 42, 56 rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Chambers et al. (US-20020078408 A1).

Claims 14, 28, 42, 56:

Miner teaches that the test controller 580 generates a defect map and determine the correct way to repair the array. (col. 10, lines 58-60). Chambers teaches of an error register which indicates that when errors exist, the computer system interrogates the error register at step 1120 and retrieves the stored contents of the read registers (step 1130). At this point, the test procedure terminates in a FAIL (step 1150). (Page 3, paragraph 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made that to terminate the testing procedure upon encountering an error to create a defect map. The artisan would have been motivated when creating the defect map of Miner the test procedure would terminate in a fail as taught in Chambers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703)305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703)305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

JJT

CHRISTINE T. TU
Primary Examiner